CLAIMS

What is claimed is:

1. A cache unit comprising:

a first memory tower, having a first way sub-tower and a second way sub-tower;

a second memory tower, having a first way sub-tower and a second way sub-tower; and

wherein a first cache line of the cache unit includes a first plurality of data segments in the first way sub-tower of the first memory tower and a second plurality of data segments in the first way sub-tower of the second memory tower.

2. The cache unit of Claim 1, wherein

the first cache line comprises sequential data segments;

the first plurality of data segments includes a first data segment and a third data segment; and

the second plurality of data segments includes a second data segment and a fourth data segment.

3. The cache unit of Claim 1, wherein a second cache line of the cache unit includes a first plurality of data segments in the second way sub-tower of the first memory tower and a second plurality of data segments in the second way sub-tower of the second memory tower.

4. The cache unit of Claim 3, wherein a physical line of the first memory tower includes data segments from the first cache line and the second cache line.

5. The cache unit of Claim 1, further comprising a first way multiplexer having a first input port coupled to the first way sub-tower of the first memory tower, a second input port coupled to the first way sub-tower of the first memory port; and an output port.

6. The cache unit of Claim 5, further comprising a second way multiplexer having a first input port coupled to the first way sub-tower of the second memory tower, a second input port coupled to the first way sub-tower of the second memory port; and an output port.

7. The cache unit of Claim 5, further comprising a tag unit coupled to control the first way multiplexer and the second way multiplexer.

8. The cache unit of Claim 7, wherein the tag unit is configured to determine whether a memory address is cached by the cache unit.

9. The cache unit of Claim 5, further comprising a data aligner coupled to the output port of the first way multiplexer and the output port of the second way multiplexer.

10. The cache unit of Claim 1, wherein the first memory tower further comprises a third way sub-tower and a fourth way sub-tower.

11. The cache unit of Claim 1, further comprising a third memory tower and a fourth memory tower.

12. The cache unit of Claim 11, wherein the first cache line includes a third plurality of data segments in the third memory tower and a fourth plurality of data segments in the fourth memory tower.

13. A method of operating a cache unit having a first memory tower and a second memory tower, the method comprising:

storing a first plurality of data segments of a first cache line in a first way sub-tower of the first memory tower;

storing a second plurality of data segments of the first cache line in a first way sub-tower of the second memory tower;

storing a first plurality of data segments of a second cache line in a second way sub-tower of the first memory tower; and

storing a second plurality of data segments of the second cache line in a second way sub-tower of the second memory tower.

14. The method of Claim 13, further comprising:

activating a first physical line of the first memory tower, wherein the first physical line includes data segments from the first cache line and the second cache line; and

activating a second physical line of the second memory tower, wherein the second physical line of the second memory tower includes data segments from the first cache line and the second cache line.

15. The method of Claim 14, wherein the first physical line of the first memory tower has a different address than the second physical line of the second memory tower.

16. The method of Claim 15, wherein a first data segment of the first cache line is in the first way sub-tower of the first memory tower and a second data segment of the first cache line is in the first way sub-tower of the second memory tower and wherein the second data segment is adjacent the first data segment.

17. The method of Claim 15, wherein the first data segment is in the first physical line of the first memory tower and the second data segment is in the second physical line of the second memory tower.

18. The method of Claim 17, further comprising realigning the first data segment and the second data segment.

19. A cache unit having a first memory tower and a second memory tower, comprising:

means for storing a first plurality of data segments of a first cache line in a first way sub-tower of the first memory tower;

means for storing a second plurality of data segments of the first cache line in a first way sub-tower of the second memory tower;

means for storing a first plurality of data segments of a second cache line in a second way sub-tower of the first memory tower; and

means for storing a second plurality of data segments of the second cache line in a second way sub-tower of the second memory tower.

20. The cache unit of Claim 19, further comprising:

means for activating a first physical line of the first memory tower, wherein the first physical line includes data segments from the first cache line and the second cache line; and

means for activating a second physical line of the second memory tower, wherein the second physical line of the second memory tower includes data segments from the first cache line and the second cache line.

21. The cache unit of Claim 20, wherein the first physical line of the first memory tower has a different address than the second physical line of the second memory tower.

22. The cache unit of Claim 21, wherein a first data segment of the first cache line is in the first way sub-tower of the first memory tower and a second data segment of the first cache line is in the first way sub-tower of the second memory tower and wherein the second data segment is adjacent the first data segment.

23. The method of Claim 21, wherein the first data segment is in the first physical line of the first memory tower and the second data segment is in the second physical line of the second memory tower.

24. The cache unit of Claim 23, further comprising means for realigning the first data segment and the second data segment.